S.No.: 202

No. of Printed Pages: 04

Following Paper ID and Roll No. to be filled in your Answer Book.		
PAPER ID: 33218	Roll No.	

B. Tech. Examination 2021-22

(Even Semester)

COMPUTER ORGANIZATION & ARCHITECTURE

Time: Three Hours] [Maximum Marks: 60

Note: - Attempt all questions.

SECTION-A

1. Attempt all parts of the following: $8 \times 1 = 8$

- (a) What do you mean by register?
- (b) How many types of buses are there?
- (c) Explain two logical micro operations.
- (d) What is meant by instruction?
- (e) What is synchronous communication?
- (f) What is an I/O interface?

- (g) What is cache memory?
- (h) Define memory access time.

SECTION-B

- 2. Attempt any two parts of the following: $2 \times 6 = 12$
 - (a) Draw the flow chart and explain about booths algorithm. Multiply 100111 with 11011 using booths algorithm.
 - (b) What is the difference between a hardwired control design and a microprogrammed control design?
 - (c) What do you mean by interrupts? Explain different types of interrupts.
 - (d) What do you mean by memory hierarchy? Why such hierarchy is required? Draw a suitable memory hierarchy block diagram with the parameters you have considered.

SECTION-C

- Note: Attempt all questions. Attempt any two parts from each questions. $5\times8=40$
- 3. (a) Explain briefly the Von-Neumann architecture.

- (b) Illustrate the register transfer mechanism for P: R2 ← R1 with necessary diagram.
- (c) Define briefly the bus arbitration technique.
- 4. (a) What do you mean by microinstruction sequencing?
 - (b) What is instruction piplines? Also explain the performance of pipeline.
 - (c) Define the following:
 - (i) Micro instruction
 - (ii) Micro-program
- 5. (a) Write short notes on programmed I/O and interrupt initiated I/O.
 - (b) What is the difference between I/O interface and I/O port.
 - (c) With a neat schematic, explain about DMA controller and its mode of data transfer.
- 6. (a) Write about auxiliary memory devices.
 - (b) Explain the mechanism involved in magnetic disk and magnetic tapes.

(c) Illustrate the mapping process involved in transformation of data from main memory to cache memory.
